IN THE CLAIMS

Please amend the claims as follows:

1. (original) A Finite Impulse Response (FIR) filter device for sample rate converting a sequence of discrete representations; the filter device including:

- an input pipeline IP for receiving the sequence of discrete representations and including:

- a sequence of input delay cells DI_i, each for storing a discrete representation; and

- a plurality of *N* input tap points TP_i, where an input tap point is provided at least between each sequential pair of input delay cells;

- an output pipeline for supplying a sequence of discrete representations and including:

- a sequence of output delay cells DO_i, each for storing a discrete representation;

- a plurality of *N* summating elements S_i for adding at least two discrete representations, a summating element being provided at least between each sequential pair of output delay cells; and

- an output switching network OSN for accumulating output values from the summating elements; and

- a sequence of N taps T_i for coupling the input pipeline to the output pipeline; each tap including a respective multiplier M_i for multiplying a discrete representation from an input tap point by a coefficient; at least N-1 of the taps including a switching element for directing a discrete representation from an input tap point through the multiplier to a summating element; the switching elements being arranged to enable supply of a discrete representation from any tap point TP_j to a summating element Si, where j <=i.

2. (original) A FIR filter device as claimed in claim 1, wherein each of the taps T_i are coupled to only one respective summating elements S_i; the switching element SW_i being provided in between tap points TP_j, where j <=i and the multiplier M_i.

3. (original) A FIR filter device as claimed in claim 1, having a constant filter width N, N output delay cells DO_i, and N or N-1 input delay cells DI_i.

4. (original) A FIR filter device as claimed in claim 1, wherein the input pipeline includes a input switching network ISN for accumulating input values in the input delay cells DI_i.

5. (original) A FIR filter device as claimed in claim 1, wherein each multiplier M_i is associated with a respective coefficient matrix C_i to enable poly-phase filtering.

6. (original) A FIR filter device as claimed in claim 1, including a controller operative to control the filter device based on a state machine.

7. (original) A FIR filter device as claimed in claim 1, wherein the state machine determines at least one of the following:

- a setting of the switching elements SWi,
- a setting of the output switching network,
- clocking of the input pipeline and/or output pipeline.

8. (currently amended) A FIR filter device as claimed in claim 5 ~~and 7~~, wherein the state machine determines selection of a coefficient from the coefficient matrix C_i.

9. (currently amended) A FIR filter device as claimed in claim 4 ~~and 7~~, wherein the state machine determines a setting of the input switching network.

10. (original) A FIR filter device as claimed in claim 1, including a further delay element and a subtracting element for determining a difference between an input discrete element and an immediately preceding input discrete element and supplying the difference into the input pipeline; and including a further summating element for adding input discrete element or the immediately preceding input discrete element to an output discrete element to be supplied by the output pipeline.

11. (original) A signal processing apparatus including a FIR filter device as claimed in claim 1 for sample rate converting an input signal, where the discrete representation is a sampled input signal, for subsequent rendering by a rendering device.

12. (original) A signal processing apparatus as claimed in claim 11, wherein the signal processing apparatus includes the rendering device.